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INF	ORMATI	ON DIS	CLOSURE	Filing Date 08/18/03		
STATEMENT BY APPLICANT			PPLICANT	First Named Inventor	James H. Kukula	
	fice se mon	ny sheets as ne		Art Unit	2825	
	(Ose as man	ly allects as in	cessery)	Examiner Name	ROSSOSHEK, YELENA	
Sheet	1	of	1	Attorney Docket Number	SNPS 0504	

Examiner Cite Initials* Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. HR Representing circuits more efficiently in symbolic model checking.* Burch, J.R.; Clarke, E.M.; Long, D.E. ACM/IEEE 28th Design Automation Conference, 1991. Publication Date: June 17-21, 1991. On page(s): 403 – 407. Efficient Model Checking by Automated Ordering of Transition Relation Partitions.* Daniel Gelst., Ilan Beer. Proceedings of the 6th International Conference on Computer Aided Verification. Publication Date: June 21-23, 1994. On page(s): 299-310. Early quantification and partitioned transition relations.* Hojati, R.; Krishnan, S.C.; Brayton, R.K. Proceedings, IEEE International Conference on Computer Design (ICCD): VLSI in Computers and Processors, 1996. Publication Date: 7-9 Oct. 1996. On page(s): 12 - 19. Border-Block Triangular Form and Conjunction Schedule in Image Computation.* In-Ho Moon, Gary D. Hacktel, Fabio Somenzi. Proceedings of the Third International Conference on Formal Methods in Computer-Aided Design. Publication Date: November 01-03, 2000. On page(s): 73-90. Efficient BDD algorithms for FSM synthesis and verification.* R. K. Ranjan, A. Aziz, R. K. Brayton, B. F. Plessier, and C. Pixley. International Workshop for Logic Synthesis, May 1995. Lake Tahoe, CA. Implicit state enumeration of finite state machines using BDD's.* Touati, H.J., Savoj, H., Lin, B., Brayton, R.K. and Sangjovanni-Vincentelli, A. IEEE International Conference on Computer-Aided Design (ICCAD), 1990. Digest of Technical Papers. Publication Date: 11-15 Nov. 1990. On page(s): 130 – 133.		T	NON PATENT LITERATURE DOCUMENTS		
ACM/IEEE 28th Design Automation Conference, 1991. Publication Date: June 17-21, 1991. On page(s): 403 – 407. "Efficient Model Checking by Automated Ordering of Transition Relation Partitions." Daniel Geist , Ilan Beer. Proceedings of the 6th International Conference on Computer Aided Verification. Publication Date: June 21-23, 1994. On page(s): 299-310. "Early quantification and partitioned transition relations." Hojati, R.; Krishnan, S.C.; Brayton, R.K. Proceedings, IEEE International Conference on Computer Design (ICCD): VLSI in Computers and Processors, 1996. Publication Date: 7-9 Oct. 1996. On page(s): 12 - 19. "Border-Block Triangular Form and Conjunction Schedule in Image Computation." In-Ho Moon , Gary D. Hachtel , Fabio Somenzi. Proceedings of the Third International Conference on Formal Methods in Computer-Aided Design. Publication Date: November 01-03, 2000. On page(s): 73-90. "Efficient BDD algorithms for FSM synthesis and verification." R. K. Ranjan, A. Aziz, R. K. Brayton, B. F. Plessier, and C. Pixley. International Workshop for Logic Synthesis, May 1995. Lake Tahoe, CA. "Implicit state enumeration of finite state machines using BDD's." Touati, H.J., Savoj, H., Lin, B., Brayton, R.K. and Sangiovanni-Vincentelli, A. IEEE International Conference on Computer-Aided Design (ICCAD), 1990.					
Proceedings of the 6th International Conference on Computer Aided Verification. Publication Date: June 21-23, 1994. On page(s): 299-310. *Early quantification and partitioned transition relations.* Hojati, R.; Krishnan, S.C.; Brayton, R.K. Proceedings, IEEE International Conference on Computer Design (ICCD): VLSI in Computers and Processors, 1996. Publication Date: 7-9 Oct. 1996. On page(s): 12 - 19. *Border-Block Triangular Form and Conjunction Schedule in Image Computation.* In-Ho Moon, Gary D. Hachtel, Fabio Somenzi. Proceedings of the Third International Conference on Formal Methods in Computer-Aided Design. Publication Date: November 01-03, 2000. On page(s): 73-90. *Efficient BDD algorithms for FSM synthesis and verification.* R. K. Ranjan, A. Aziz, R. K. Brayton, B. F. Plessier, and C. Pixley. International Workshop for Logic Synthesis, May 1995. Lake Tahoe, CA. *Implicit state enumeration of finite state machines using BDD's.* Touati, H.J., Savoj, H., Lin, B., Brayton, R.K. and Sanglovanni-Vincentelli, A. IEEE International Conference on Computer-Aided Design (ICCAD), 1990.	HR L	1	ACM/IEEE 28th Design Automation Conference, 1991. Publication Date: June 17-21, 1991. On page(s): 403 -		
3 IEEE International Conference on Computer Design (ICCD): VLSI in Computers and Processors, 1996. Publication Date: 7-9 Oct. 1996. On page(s): 12 - 19. "Border-Block Triangular Form and Conjunction Schedule in Image Computation." In-Ho Moon, Gary D. Hachtel, Fabio Somenzi. Proceedings of the Third International Conference on Formal Methods in Computer-Aided Design. Publication Date: November 01-03, 2000. On page(s): 73-90. "Efficient BDD algorithms for FSM synthesis and verification." R. K. Ranjan, A. Aziz, R. K. Brayton, B. F. Plessier, and C. Pixley. International Workshop for Logic Synthesis, May 1995. Lake Tahoe, CA. "Implicit state enumeration of finite state machines using BDD's." Touati, H.J., Savoj, H., Lin, B., Brayton, R.K. and Sangiovanni-Vincentelli, A. IEEE International Conference on Computer-Aided Design (ICCAD), 1990.		2	Proceedings of the 6th International Conference on Computer Aided Verification. Publication Date: June 21-23,		
Hachtel , Fabio Somenzi. Proceedings of the Third International Conference on Formal Methods in Computer-Aided Design. Publication Date: November 01-03, 2000. On page(s): 73-90. "Efficient BDD algorithms for FSM synthesis and verification." R. K. Ranjan, A. Aziz, R. K. Brayton, B. F. Plessier, and C. Pixley. International Workshop for Logic Synthesis, May 1995. Lake Tahoe, CA. "Implicit state enumeration of finite state machines using BDD's." Touati, H.J., Savoj, H., Lin, B., Brayton, R.K. and Sanglovanni-Vincentelli, A. IEEE International Conference on Computer-Aided Design (ICCAD), 1990.		3 ·	IEEE International Conference on Computer Design (ICCD): VLSI in Computers and Processors, 1996.		
Plessier, and C. Pixley. International Workshop for Logic Synthesis, May 1995. Lake Tahoe, CA. "Implicit state enumeration of finite state machines using BDD's." Touati, H.J., Savoj, H., Lin, B., Brayton, R.K. and Sangiovanni-Vincentelli, A. IEEE International Conference on Computer-Aided Design (ICCAD), 1990.		4	Hachtel, Fabio Somenzi. Proceedings of the Third International Conference on Formal Methods in		
6 and Sangiovanni-Vincentelli, A. IEEE International Conference on Computer-Aided Design (ICCAD), 1990.	$\sqrt{}$	5			
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